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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,019	12/07/2001	Francesco Pessolano	NL 000667	8972

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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,019	PESSOLANO ET AL.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11 and 13-14 have been examined.

2. Acknowledgement of papers filed: Appeal Brief 9/20/2005.

Withdrawn Rejections

3. Applicant, via arguments, has overcome the rejections to claims 1-2, 5-11 and 13-14 set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the Examiner.

Maintained Objections

4. Applicant has not overcome or addressed the objection to claim 5 set forth in the previous Office Action. Therefore, this objections is respectfully maintained by the examiner and copied below for applicant's convenience.

5. As per claim 5, 5. the limitation recites an apparatus according to "any one of claim 2" in line 1 of the claim. Please amend the claim language to read, "An apparatus according to claim 2" or the like in order to clarify the claim.

New Objections

6. Claims 2, 3 are objected to for the following grammatical/typographical error: "(first-in/***fist***-out)". Appropriate correction is required.

Maintained Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 recite the limitation, "An apparatus according to claim 10" in the first line of the claim. There is insufficient antecedent basis for this limitation in the claim, as the claim depends from a method claim. Therefore, the claim will be interpreted as reciting the limitation "A method according to claim 10" for the purpose of this office action.

Maintained Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by White et al., U.S. Patent 5,632,023, herein referred to as White.

11. As per claim 3, White has taught a digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units [235, 240, 245, 260 and 265 of Figure 2B] wherein each functional unit is adapted to execute operations [It is inherent that each functional unit is adapted to execute operations], and

control means for controlling said functional units in coordination with one another [235R, 240R, 245R, 260R and 265R of Figure 2B, each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available (col. 11, lines 36-47), thereby controlling its function] in response to a single fetch unit [230 of Figure 2A] and a single decode unit [210 of Figure 2A], characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units [285 of Figure 2A, the Reorder Buffer is a FIFO register (register meaning a device capable of retaining information of the aggregate information in a digital computer) device which is utilized by all of the functional units to support data-flow, in that the functional units can use the data before it is committed to the register file. As stated in the previous Final Action, White explicitly states the Reorder Buffer is a FIFO buffer, "Reorder buffer 285 is managed as a first-in first-out (FIFO) device." (***Col. 11, lines 21-22***)].

New Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Superscalar Microprocessor Design, by Mike Johnson, herein referred to as Johnson..

14. As per claim 3, Johnson teaches a digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units (fig. 3-7, Branch, ALU, Shifter, Load and Store) wherein each functional unit is adapted to execute operations (inherent), and control means (fig. 3-7, Reservation stations at the input of every functional unit, page 46, second full paragraph) for controlling said functional units in coordination with one another (Reservation stations control the issuing of instructions when their associated operands become available because other functional units have produced them as results), which come in response to a single fetch unit and a single decode unit (Figure 3-7, page 45), characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units: The Reorder Buffer is a FIFO (Pages 92-94 and fig. 3-7 on page 45) which communicates results (data-flow) to other functional units/pending instructions in reservations stations.]

15. Claims 1-3, 5-11 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsushima.

16. As per claim 1, Tsushima teaches a digital signal processing apparatus for executing a plurality of operations, comprising

a. A plurality of functional units wherein each functional unit is adapted to execute operations, [Units 204-1, 204-2, 205-1, 205-2, 206-1, 206-2, and 207, Fig. 1]

b. And control means for controlling said functional units characterized in that said control means comprises a fetch unit, a decode unit, and a plurality of

control units responsive to said decode unit: [Instruction Fetch Unit 202, Instruction Expanding Unit 300 and Decode Unit 203 make up the control means. Small Instruction Generating Circuit 303-1 and 303-2 in each Instruction Expanding Circuit (300a-d) of the Instruction Expanding Circuit 300. (Figs. 1, 3 and 5). The Small Instruction Generating Circuits 303-1 and 303-2 receive decompressed opcodes and other control data, i.e., decoded control signals from the decode unit. While this data supplied to the Small Instruction Generating Circuits does not come from the "Decode Unit 203", the control data does come from hardware that extracts (decodes) control information/data from instructions, and thus the control data/information comes from a "Decode Unit".]

c. Wherein at least one control unit is operatively associated with a respective functional unit for controlling its function, including controlling a number of repetitions of execution of its function: [Each small instruction generator contains a "NOP Instruction Register 604, Selector 600 and a Control Circuit 620, which control the function for it's respective functional unit. The Small Instruction Generator chooses between the opcode provided by line 50-1 or a NOP instruction using the Selector, and thus controls the function of the functional unit. Furthermore, the Control Circuit 620 controls the number or repetitions of the execution of the NOP function. (Fig. 5, col. 10, lines 35-54, col. 16, line 36 to col. 17, line 28)]

d. And each functional unit is adapted to execute operations in an autonomous manner under control of the control unit associated therewith. [Each

functional unit is autonomous under control of the Control Unit 620, as a number of NOPs is encoded and delivered to the Small Instruction Generating Circuits and the Small Instruction Generating Circuit alone issues the appropriate number of NOP instructions. (Fig. 5, col. 10, lines 35-54, col. 16, line 36 to col. 17, line 28)]

17. As per claim 2, Tsushima teaches an apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units: [The operand queues 302-1 and 302-2 of each Instruction Expanding Circuit (300a-d) are each FIFO register means adapted for supporting data-flow communication among said functional units. From a first point of view, data flows from each queue to the associated functional unit, which is an example of communication among functional units. From a second point of view, the opcodes sent from the queues 302-1 and 302-2 include, for instance, load instructions. Load instructions are executed by the load/store functional unit and load data from memory to registers, which other functional units then use. Therefore, one FIFO queue is supporting communication between the load/store functional unit and the other functional units. Figures 1 and 3, col. 16, lines 27-35.]

18. As per claim 3, Tsushima teaches a digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units [Units 204-1, 204-2, 205-1, 205-2, 206-1, 206-2, and 207, Fig. 1] wherein each functional unit is adapted to execute operations, and control means for controlling said functional units in coordination with one another in response to a single fetch unit (Figure 1, Fetch Unit

202) and a single decode unit (Decode Unit 203), characterized by FIFO (first-in/first-out) register means (The operand queues 302-1 and 302-2 of each Instruction Expanding Circuit (300a-d)) adapted for supporting data-flow communication among said functional units: [The operand queues 302-1 and 302-2 of each Instruction Expanding Circuit (300a-d) are each FIFO register means adapted for supporting data-flow communication among said functional units. From a first point of view, data flows from each queue to the associated functional unit, which is an example of communication among functional units. From a second point of view, the opcodes sent from the queues 302-1 and 302-2 include, for instance, load instructions. Load instructions are executed by the load/store functional unit and load data from memory to registers, which other functional units then use. Therefore, one FIFO queue is supporting communication between the load/store functional unit and the other functional units. Figures 1 and 3, col. 16, lines 27-35.]

19. As per claim 5, Tsushima teaches an apparatus according to any one of claims 2, characterized in that said FIFO register means comprises a plurality of FIFO registers: [The operand queues 302-1 and 302-2 are FIFOs that are made up of registers. Since the registers are part of a FIFO queue, they are FIFO registers. Figures 1 and 3, col. 16, lines 27-35.]

20. As per claim 6, Tsushima has taught an apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit: [Each functional unit has an associated Small Instruction Generating Circuit 303-1 or 303-2 (figs. 1, 3 and 5).]

21. As per claim 7, Tsushima has taught an apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage comprises a functional unit [Fig. 1, the pipelines includes at least a Fetch stage, expanding stage, decode stage, execution stage (functional units) and write back stage (functional units to register file).]

22. As per claim 8, Tsushima has taught an apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, wherein said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit [Figure 5, Counter 601 and NOP Instruction Register 604].

23. As per claim 9, Tsushima has taught an apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units [Both Main Storage 100 and Instruction Cache 201 are memories that contain instructions, which is what controls the control circuit in the Control Units (Small Instruction Generating Circuits 303-1 and 303-2. Figs. 1 and 5, col. 6, liens 1-9 and col. 16, lines 27-35.]

24. As per claim 10, given the similarities between claim 1 and claim 10, the arguments in the rejection of claim 1 also apply to claim 10.

25. As per claim 11, given the similarities between claim 2 and claim 11, the arguments in the rejection of claim 2 also apply to claim 11.

26. As per claim 13, given the similarities between claim 7 and claim 13, the arguments in the rejection of claim 7 also apply to claim 13. Examiner also notes that

each of the stages is executed by a functional unit, e.g., the fetch unit is a functional unit because it's function is performing instruction fetches.

27. As per claim 14, given the similarities between claim 8 and claim 14, the arguments in the rejection of claim 8 also apply to claim 14.

Response to Arguments

28. Applicant's arguments filed on 9/20/2005 in regards to claims 1-2, 5-11 and 13-14 have been fully considered but they are found moot in view of the new rejections.

29. Applicants arguments filed on 9/20/2005 in regards to claim 3 have been fully considered but they are not persuasive.

30. Applicant argues the novelty/rejection of claim 3:

> "With respect to claim 3, which was previously presented, the rejections describes 'FIFO...register means adapted for supporting data-flow communication among said functional units [285 of Figure 2A, the Reorder Buffer is a FIFO register...device which is utilized by all of the functional units to support data-flow....'
>
> Applicant respectfully disagrees. There is no indication in White that the Reorder Buffer of White is a FIFO register. Typically, the Reorder Buffer of White would not be expected to be realized using a FIFO register."

31. These arguments are not found persuasive for the following reasons:

e. To clarify, applicant's attention is directed towards the previous response to this argument, which was set forth in the Final Action mailed 4/21/2005 and is copied below for Applicant's convenience.

i. ***"The reorder buffer of White is a FIFO buffer (col. 11, lines 21-22) with a plurality of entries.*** Given that the definition of a register is "a device capable of retaining information of the aggregate information in a digital computer', the FIFO buffer is a FIFO register means." (Final Action, mailed 4/21/2005, page 10.)

f. Furthermore, the cited portion of White is copied below for Applicant's convenience:

ii. ***"Reorder buffer 285 is managed as a first-in first out (FIFO) device."*** (White, Col. 11, lines 21-22).

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

EDDIE CHAN
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